REMARKS

I. 35 U.S.C § 112

There was an error in claim 2 and this has been corrected it the enclosed amendments.

II. 35 U.S.C. §.103

The Examiner takes the view that it would have been natural to use the testing method of *Folea* to test the circuit of *Lulla,* which has a circuit 102 with JTAG support and a circuit 104 without JTAG support.

Folea describes (see abstract) a system for monitoring and controlling boundary scan chains – i.e. boundary scan capable devices or chains of boundary scan capable devices. *Folea* makes reference to a "device under test (DUT)" – see col. 3, lines 52 to 59 – which clearly means a single IC. It is clear from col. 4, lines 36-41 that for every DUT there is a BSDL file. This means that all DUTs are JTAG-capable. *Folea* also makes reference to "devices under test" (col. 3, lines 59-63) (emphasis added) and testing "integrated circuits and systems" (col. 1, lines 16-22), but the overall disclosure is that where anything more than a single device is to be tested, it is a chain or plurality of JTAG capable devices that are to be tested. Nowhere is there any hint or suggestion that testing can be performed of a combination of JTAG and non-JTAG devices on a common circuit.

Lulla describes a combination of a JTAG device and a non-JTAG device. *Lulla* describes an embodiment with two chips in a single IC package and an embodiment with two chips on a circuit board. Accordingly, if one is to consider (as the Examiner does) using the method of *Folea* to test "the circuit" of *Lulla* (and the Applicant makes no admission that it would be obvious to do so without the benefit of hindsight), the Examiner must be specific as to which embodiment of *Lulla* is to be considered.

The first embodiment (two chips in a single IC package) is a single JTAG device. Applying *Folea* to test this embodiment of "the circuit" of *Lulla* does not arrive at the claimed invention.

The Applicant therefore assumes that the Examiner is considering applying the method of *Folea* to the second embodiment of *Lulla*.

The Examiner takes the view that a conventional net list file would be necessary for testing the non-JTAG circuit 104. The Applicant disagrees. First, the "netlist" in the case of the circuit of *Lulla* is trivial – it is merely an address bus, a data bus and three output pins of circuit 102 connected to corresponding pins of circuit 104. It is too trivial to merit providing as a file, and certainly too trivial to suggest that such a file should be parsed or analyzed. Second, the circuit of *Lulla* is specifically designed so that the connections between the circuit 102 and memory 104 are fixed and well defined (i.e. there is no netlist). The programming is achieved by adding a extra register ("NV" register) in the JTAG scan chain which holds address, data and control pin information. In other words, circuit 102 already has the "knowledge" about how to read and write the memory, and the JTAG bus is used to control it. There is no need for a netlist and certainly no need to parse or analyze a netlist.

The Examiner contends that *Folea* teaches running scripts. The Applicant disagrees. The Applicant's representative has scanned the text and can find no reference to any script. Neither is there any equivalent, because *Folea* describes a tool for manual testing of a JTAG capable device or chain of such devices. The Examiner acknowledges that testing is manual.

The Examiner makes reference to col. 5, lines 38-42 as "initiating a script" but these lines merely describe a scan of the components in a mode selected by the user. This is not a test script.

Folea makes reference to 'test vectors' and 'test executives' in the section "Background of the Invention" at col 1, lines 54-61. A test executive is used to apply the test vectors to test connections between JTAG devices. A program which takes a BSDL files and a netlist (and maybe other information) can be used to automatically generate the test vectors. This is called an Automatic Test Pattern Generator or ATPG for short. At col. 1, lines 61-64 it is explained how known tools at that time "have a steep

learning curve and require a fundamental understanding of boundary scan that most design engineers do not have." Furthermore, col. 1 line 64- col. 2, line 2 describes how test points and probes must be added to cover components that are not boundary scan capable. *Folea* teaches away from the use of such techniques by instead providing a manual tool that facilitates testing.

The Examiner points to col. 3, lines 11-14 where it is stated that the tester of *Folea* does not replace the prior art, but rather augments it. We must be careful just how much we read into such a statement. The Examiner concludes "in other words, *Folea* recognizes the necessity of the prior art methods of using a netlist for testing devices." As an initial observation, the Applicant contends that this particular assumption cannot be drawn, but more generally, the Applicant submits the following comments on the "teaching away" by *Folea*.

Col. 2, lines 43-46 says that *Folea* "overcomes the above noted issues of the prior art by providing a method and apparatus that does not require the use of test vectors, test executives, netlists or schematics to run boundary scan operations . . ." Thus, *Folea* teaches away from using four things that make the prior art excessively complicated: test vectors, test executives, netlists and schematics.

Moreover, even the "augmentation" of the use of test vectors, test executives, netlists and schematics with the teaching of *Folea* does not overcome the problem of testing components that are not boundary scan capable. *Folea* does not explain how to address the problem of testing connections to components that are not boundary scan capable without the use of additional test points and probes. *Folea* concedes that these create additional costs and complications but does not overcome these costs and complications. If *Folea* provides a solution (to the costs and complications), it is a mere manual solution with an improved user interface. *Folea* still cannot provided automated testing of components that are not boundary scan capable without the use of additional test points and probes.

The present invention addresses the complexity problem in a different way and extends the testing to non-JTAG components independent of how they are connected to the JTAG components, i.e. without any presumption that the JTAG components have registers (as in *Lulla*) for connection to the non-JTAG components.

The present system uses a 'script' to generate test vectors. The test vectors can be generated for a particular non-JTAG device (the Applicant calls this "device-centric" testing) irrespective of the circuit in which it is being used. In other words, the test script is specifically for testing the second IC. Complexity is avoided, because a chip supplier can provide a script specific to the IC and all the test engineer has to do is provide the boundary scan file and the netlist. The invention does the rest. It parses and analyzes the BSDL file, the netlist and the connections list to find points from which selected pins of the second IC can be driven and read via the first IC, and it generates a data structure therefrom which permits automated execution of the test script from the computer through the boundary scan bus whereby the interconnections between the first IC and the second IC can be tested.

A script can generate test vectors in real-time. The great advantage of this is that different test vectors can be generated depending on the result of the application of the previous test vector.

Folea is explicitly intended for a system where executing test vectors is not required, mainly because it does no real testing. Thus the manual tool of *Folea* could not, without improper hindsight modification, practically be used to test interconnects between a JTAG device and a non-JTAG device, because it would take a lifetime and more to devise and manually execute all the necessary steps to test the interconnections between two such devices using the tool of *Folea*. Consider, by way of example, the testing of interconnects from a circuit such as circuit 102 of *Lulla* to a memory such as memory 104 of *Lulla*. To test the interconnects, one needs a test script to test a memory (an example of a test script that is *specific to the second IC* as claimed in claim 1, or *specific to the second IC but independent of the first*

IC as claimed in claim 8). For example, it is not enough that such a test script merely writes data to a memory location, reads data back from the same memory location,checks that the data read back is the same as the data written in, and repeats for the next memory location, because such a simple three-step test does not test the possibility that the right data is written to the wrong address, nor the possibility that, due to a short between address lines, the same data is written to more than one address. The memory circuit 104 of *Lulla* has 18 address lines. So to test the interconnections, one also needs to read back from a very large number of other addresses to see if the same data has been written to another address.

The Examiner contends that the "test script" of *Folea* is independent of the JTAG device, and references col. 5, lines 28-32 (office action, page 12[1]), but this paragraph in *Folea* does not refer to test scripts. It merely refers to a scan, i.e. a single boundary scan operation. Moreover, the Examiner is taking the claim element *test script* out of its context in the claims. Claim 1 calls for a test script that is *specific to the [non-JTAG] IC.* Claim 8 calls for a test script that is *specific to the [non-JTAG] IC but independent of the [JTAG] IC.*

All *Folea* teaches is a tool to allow the test engineer to take control of the JTAG pins.

Additionally, or in the alternative, a person of ordinary skill in the art would not consider using the tool and method of *Folea* to test the interconnects between the two circuits of *Lulla*, because to do so would be unduly time consuming using the manual tool of *Folea*.

In discussing *Lulla*, the Examiner says[2] "*Lulla* further teaches the equipment of claim 1 for testing the first pin (Fig 1, element 122) of a first device of the circuit to be tested". It has already been discussed that *Lulla* does not describe any testing of the non-JTAG device, and the Examiner appears not

[1] The Examiner makes reference to Fig. 5 of *Lulla* but it is believed he intends to reference Fig. 5 of *Folea*
[2] At the foot of page 8 of the Office Action

to contest this point, merely indicating that he does not consider it relevant to his argument in applying the testing to *Folea* to the circuit of *Lulla*.

There is a reference in *Lulla* to "testing" at column 1, lines 45 to 48, and the Examiner considers that this reference teaches "the second IC and its connections to the first IC can be tested by driving pins of the first IC" (office action, page 11), but these lines in *Lulla* merely describe that a JTAG-capable PLD can be tested using a JTAG bus. These lines describe the background to *Lulla*. The Examiner cannot take them out of context and allege that they refer to testing of a second IC connected to the JTAG-capable PLD.[3]

To the contrary, it is explicitly stated in *Lulla* at col. 7, lines 43 to 46, that the boundary scan register may be used to test the operation of the [JTAG compatible] circuit 102, but in contrast to using the boundary scan register, "*the NV interface register may be used to control the operation of the circuit 104*". Accordingly, it appears that the author does not believe that the circuit 104 can be tested through the boundary scan register.

Turning to *Tiong*, the Examiner believes this reference teaches a simplified method of creating BSDL and net list files (see middle of page 8 of the Office Action). He references column 3, lines 26 to 31 of *Tiong*. That passage reads as follows:

> The present invention allows the both the VERILOG net list and the BSDL files to be generated from one file of input parameters, again, eliminating a labour-intensive process. Thus the systems and methods of the present invention improve the speed,

[3] There are other references in *Lulla* to 'run-test-idle', and the Examiner has not relied on these. The 'run-test-idle' state has nothing to do with testing. It is one of the states in the JTAG tap controller. It is an idle state in which nothing happens, and its uses need not be discussed.

accuracy and simplicity of hardware description code generation, and overcome the limitations and shortcomings of the prior art.

Quite the contrary to taking a BSDL file and a net list and parsing them to generate a data structure, all *Tiong* describes is the generation of separate net lists and BSDL files.

Amended claims

In accordance with the enclosed amended claims, circuit testing equipment is provided for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable and at least one second IC that is not boundary-scan capable, and in particular for testing interconnections between the first IC and the second IC.

Folea does not teach or suggest testing interconnections between two ICs. *Folea* teaches manual testing of a chain of JTAG devices but does not mention or suggest a non-working chain, i.e. testing for a break in the chain or other fault in the interconnections between devices of the chain. Moreover, *Folea* does not teach or suggest testing interconnections between a JTAG IC and a non-JTAG IC.

The claimed equipment comprises a computer having stored thereon a boundary scan description language (BSDL) file for the first IC, and a netlist and a connections list for the circuit to be tested, and having loaded therein a test script for testing the second IC.

Folea does not teach or suggest storing a netlist and a connections list. Neither does *Folea* teach or suggest providing a test script for testing any IC, and certainly not for testing a non-JTAG IC connected to a JTAG IC. The same is true when applying *Folea* to the testing of a circuit as described by *Lulla*. Moreover, it would not be obvious for a person of ordinary skill in the art to provide a test script specifically for testing the non-JTAG circuit 104 of *Lulla* independent of JTAG circuit 102.

The claimed element of the computer is arranged to parse and analyze the BSDL file, the netlist and the connections list, to find points from which selected pins of the second IC can be driven and read via the first IC, and to generate a data structure therefrom which permits automated execution of the test script from the computer through the boundary scan bus whereby the interconnections between the first IC and the second IC can be tested.

In *Folea*, only the BSDL file is parsed (col. 4, lines 56-58). There is no netlist. Even when applied to the testing of the circuit of *Lulla*, there is still no netlist capable of being parsed (in *Lulla* there is only a table). There is no teaching or suggestion of parsing a BSDL file, together with a netlist (and a connections list). There is certainly no teaching or suggestion of parsing these for a particular result, *viz.* to find points from which selected pins of the second IC can be driven and read via the first IC. There is no teaching or suggestion that as a result of parsing a certain data structure is generated, *viz.* one that permits automated execution of the test script (specifically for the second, non-JTAG, IC) from the computer through the boundary scan bus, whereby the interconnections between the first IC and the second IC can be tested.

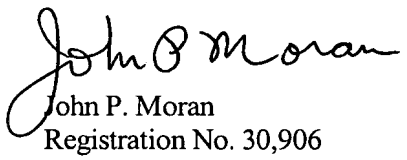
In addition to the above differences between the claims and the prior art, as claimed, the test script is specific to the second IC. This is described at page 3, lines 29 to 31, page 4, lines 13 to 19 and lines 26 to 30, and page 6, lines 24 to 28 and elsewhere. In the last mentioned passage, it is explained that a given script will serve to test only one IC, but note that the script is not specific to the board or the circuit in which the IC is mounted. In this way, an IC-specific script can be executed to test its associated IC regardless of the particular net list and connections list that defines how the IC is connected within the overall circuit to be tested. None of the prior art documents begins to address this problem. *Lulla et al*, for example, contemplates a specific combination of JTAG die and memory die for the purpose of expanding the memory available to

the first die. There is no suggestion of any test script specific to one or other die or, when the two dies are integrated in a circuit, there is no suggestion of any testing of the combined integrated circuit, so there is no need to parse any net list and/or connections list together with the BSDL file for the circuit to generate a new data structure. Neither is there any suggestion of any test script specific to the combined integrated circuit, independent of the board in which the circuit is to be mounted.

Applicant submits that the claimed invention patentability distinguishes over the prior art and respectfully requests that the Examiner reconsider and withdraw the rejections of the claims and pass this application to allowance.

If any additional fee is required in connection with this Preliminary Amendment, Applicants requests that such fee be charged to Deposit Account No. 502353.

Respectfully submitted,,



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